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VLSI ARCHITECTURE OF PACKET DELIMITERS FOR USB

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Abstract -- The Universal serial bus technology comes as a response to the increasing demands for unified interfaces and the need for flexible easy-to-use products for personal computers. Integrating this technology in to PBXs, ISDN ICs and multimedia communication systems can play an important role in the integration of telecommunication and computer technologies. The development of high-density devices with increased speed, consequently fall of per-chip costs and flexibility has made them suitable for a variety of high performance and computationally intensive applications. In this paper the hardware design approach for implementing packet delimiters function for USB in chip and this is the best solution, which reduces power requirement, size and also cost to approximately 1/N of the conventional approach.

Keywords -- VLSI, USB, ISDN, Multimedia Communication Systems

I. INTRODUCTION

The universal serial bus (USB) is an expansion scheme that replaces the serial card in PC. It provides a high-speed serial connection to the PC's bus and as many as 127 devices can be connected to the same bus [2]. Today, computer-telephone integration and video conferencing through digital cameras and computers have become a necessity in the work place and are starting to make their way into homes. These two interrelated communication functions along with future PBXs and a number of standard PC peripherals such as Key Boards, joysticks and mice, will benefit from USB usage [3-6].

USB also has features to support isochronous devices like telephone Game and Telephony device developers are particularly interested in these features. In ISDN systems. Small and medium sized private branch exchanges (PBX) represent the most evolving elements in terms of both growth and required advancements in technical features. Advanced PBXs with both telephone and datacom interfaces (i.e. Internet access) can offer significant cost benefits to their users. Where the target is the small office/home office (SOHO) systems. As an example, such a PBX could automatically select the PSTN interface (analogue or ISDN) for local telephone calls and the ‘telephony over internet' service for low-cost international calls to subscribers with similar facilities [7]. The implementation of USB functionality in such PBXs provides seamless integration between telephone and Internet applications.

The constantly increasing demand for high-speed integrated communications drives the development of advanced ISDN chip design to provide both telecom and datacom services. Telecommunications systems manufacturers and component designers face increasing demand for cheaper and more integrated products to satisfy user requests for seamless and cost-efficient service integration and network interconnectivity. Therefore a wide variety of new and existing peripherals may be developed that utilize USB.

Developer needs to ensure that their devices will operate well in combination with other devices so that end user expectations are met. Programmability and easy reconfiguration are key requirements for future ISDN systems. Developers of USB devices can determine specific details about USB from USB specification [1]. This paper present modelling and simulation of USB implementation for ISDN and multimedia communication systems in verilog HDL IEEE standard 1364.

II. USB BASIC CONCEPTS

Universal serial bus is a new personal computer (PC) interconnect that can support simultaneous attachment of multiple devices. The host serves as the master of the bus. Devices are divided into two speeds: 1.5Mbps or 12Mbps. Data transfer rate of 1.5Mbps supports low speed devices such as keyboard, mice, printer etc. Data transfer rate of 12Mbps supports wide variety of desktop peripherals such as MODEM, audio, video devices, telephones etc,[1],[8].

A USB system uses a tiered star topology where only one host exists. This host controls and initiates all transactions that occur over the USB. Devices are either directly connected to the host through the root hub or through hubs that are connected to the root hub to create a tree-like configuration [9].

The bus allows peripherals to be attached, configured, used and detached, while the host and other peripherals are in operation. USB provides facilities such as ease-of-use connectivity to the PC, flexibility and low-cost implementations. This is in addition to the 'plug and play' feature, which is one of the main reasons behind the inception of USB.

In general, USB transactions consist of up to three packets: a token packet, a data packet and a handshake packet. Each packet has a packet ID (PID) that specifies its type. A transaction starts when the host sends a token packet with a device address, and endpoint number and the direction of data transfer. The addressed device selects itself by decoding its address from the token. If the direction field in the token indicates that the host is asking for data, the device responds with a data packet, otherwise, the host follows up with the data packet. In general, after the data is received the destination (host or device) sends a handshake packet to acknowledge the reception of that packet.

III. PACKET DELIMITERS

Precise detection of packet delimiters is crucial for robust SIE operation [1]. Each packet has a start delimiter (or sync) and end delimiter (or EOP). The nominal sync field consists of an NRZI KJKJKJKK pattern. Even though this is an in band (made up of differential signals) pattern, the initial bit may be distorted due to hub turn on behavior, the DPLL may need some edges to achieve lock as well. An easy way to account for this is to use only the latter portion of the sync field to detect sync. This works because only the end of sync is needed to delimit the start of information in a packet. The sync detection can be done prior to data extraction in the DPLL. The detected end of sync will then need to be synchronized with the data stream extracted by the DPLL. It is easier and recommended to look for the end of sync in the data stream extracted by the DPLL. The pattern being searched for should comprehend that the data output from the DPLL during interpacket gap and unlocked states are not to be used when detecting the sync pattern.

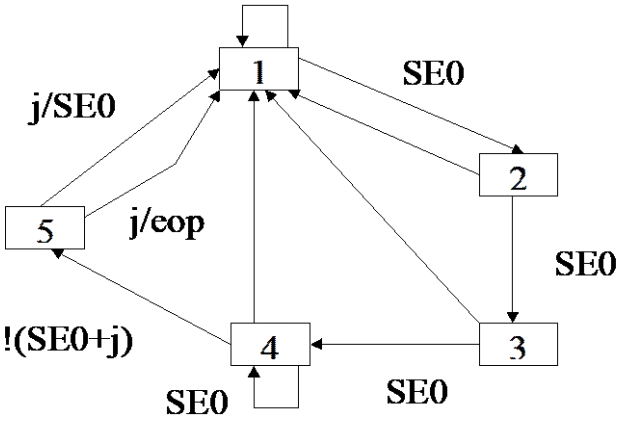

Fig 1 EOP detection state machine

One way to meet all these requirements for EOP detection is to use a state machine running in the 4x domain as shown in Fig 1.

This EOP is detected in the 4x domain; however it is used by the state machines in the 1x domain. This interdomain signaling should be analyzed carefully for race conditions.

IV. RESULTS FOR FPGA IMPLEMENTATION

Once the correctness of the design was verified, performance was analyzed. All FPGA designs were implemented using the Verilog HDL language in Xilinx ISE software.

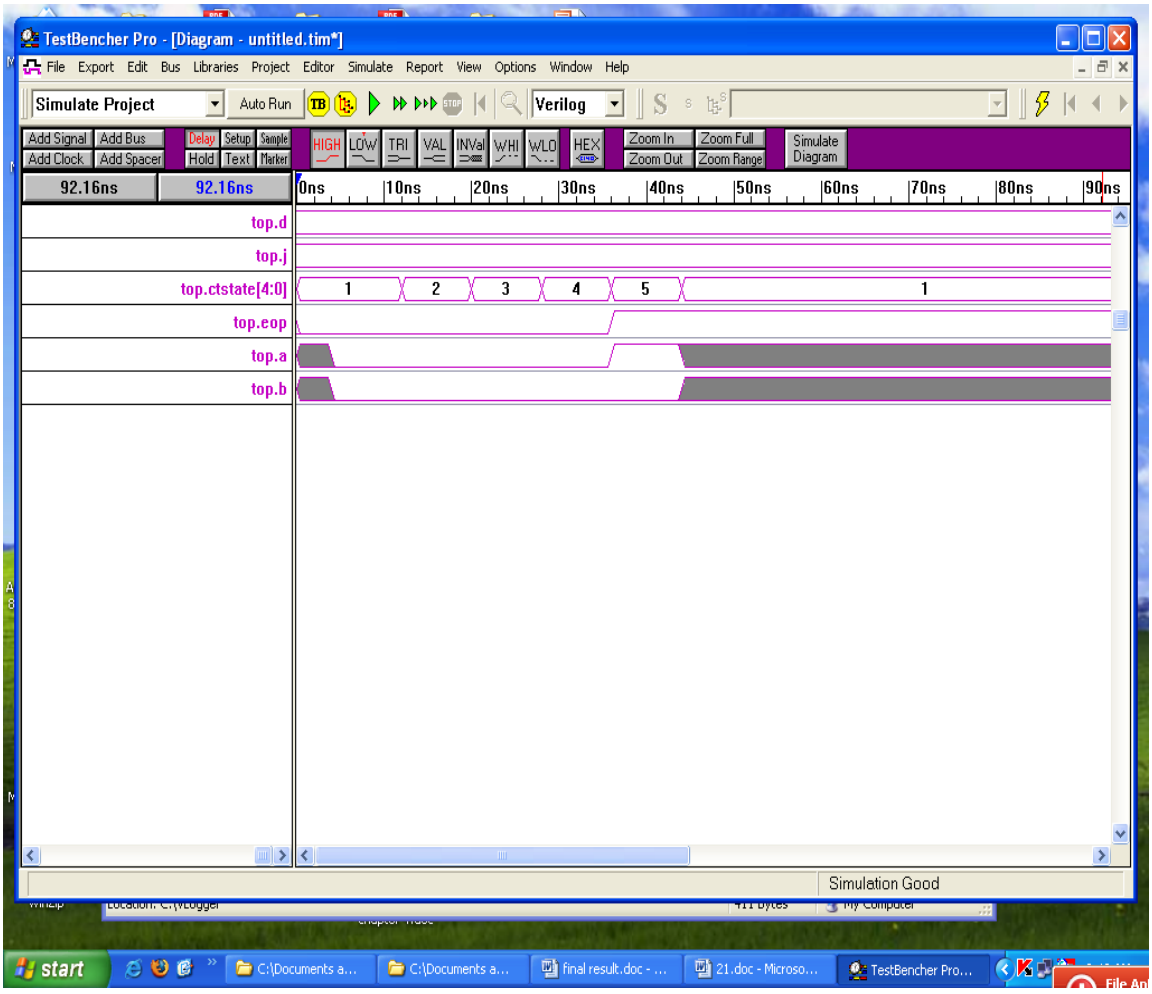

Fig. 2 Simulation timing diagram for EOP

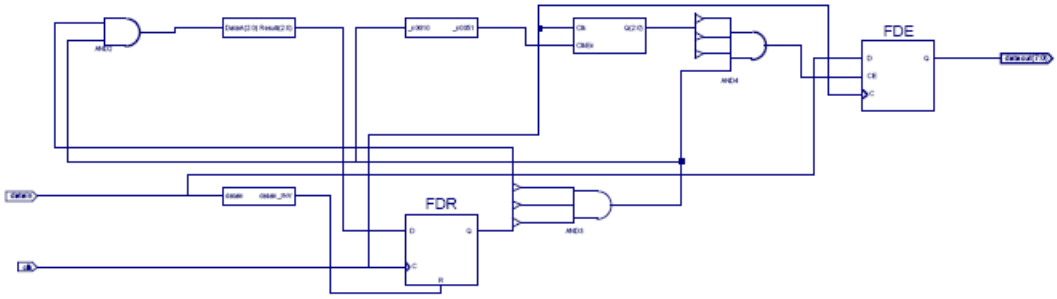

Fig. 3 Synthesis block for EOP

Fig. 2 shows the simulation timing diagram for EOP and Fig. 3 shows synthesis block for EOP

V. CONCLUSION

The benefits of this approach are mainly on the reduced IC production cost, the increased system integration and the capability to provide customised solutions. The incorporation of a packet delimiters for USB interface into IC architecture provides a number of additional capabilities such as port expansion, direct PC compatibility with ISDN and multimedia communication applications [9]. The design approach have been presented for implementing the packet delimiter functions for USB in hardware. In this paper the hardware design approach for implementing packet delimiters function for USB in chip and this is the best solution, which reduces power requirement, size and also cost to approximately 1/N of the conventional approach.

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