Self-Adaptive Configuration Frames for Addressing Permanent Errors

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Abstract-Multiple bit upsets (MBUs) and power consumption are the important parameters to be considered in field-programmable gate arrays (FPGAs). The occurrence of such MBUs will affect the functionality of the mapped design permanently. A low-cost error detection method combined with a correction scheme is an efficient approach to avoid such effects. Error detection code detects MBUs in configuration frame and the correction scheme reconstructs the erroneous configuration frame based on the concept of erasure code. The erasure code can correct only the transition errors and hence a novel in-line test (ILT) method and an improved syndrome storing-based detection (SSD) method is extended for addressing permanent errors. The ILT method uses a spare frame and the system reroutes the data of the erroneous configuration frame to the spare frame without interrupting the data flow. The total power consumed is also measured. Implementation of the design is done in VIRTEX4 family and the device used is XC4VLX25.

Keywords-Multiple bit upsets (MBUs), Field-programmable gate array (FPGA), Erasure code, In-line test (ILT), Syndrome storing-based detection (SSD).

I. INTRODUCTION

Very large scale integration (VLSI) contains more than 10^5 transistors and the parameters that can be optimized using this technology are power, area, delay, design time and testability. Field programmable gate arrays (FPGAs) are reconfigurable blocks, which plays a crucial role in many applications such as telecommunication, digital signal processing, scientific computing etc. The Virtex families are considered as legacy devices and they are based on configurable blocks where each block is equivalent to multiple ASIC gates. The Virtex-4 families are not recommended to use in new designs, although they are still produced by Xilinx for existing designs.

Multiple bit upsets (MBUs) in configuration frames are more important to be considered than the single event upsets (SEUs) and hence it requires detecting and correcting of multiple errors in memory cells. Defect-tolerant FPGA switch block and connection block architecture tolerate increasing of errors but it consumes more area [1]. Interleaved-n dimensional (InD) parity technique is one of the error-detection techniques which use parity bits to detect MBUs and less time consuming when compared to other techniques [2]-[3]. Interleaving 3 dimensional (I3D) parity uses three parity bits such as vertical, horizontal and diagonal for the error detection purpose. The techniques like low-density parity-check erasure code [4]-[8], generally target for transient errors rather than permanent errors. An effective erasure code encodes k blocks into n blocks such the original message can be reconstructed from the encoded data. Erasure code stores the parity of configuration frames to a redundant block and hence if a frame is corrupted the original message can be reconstructed with the use of the redundant block. Power gating technique provides one power gate for each cluster to reduce the total power consumption.

In order to detect and bypass permanent errors in configuration frames, a novel in-line test (ILT) method using a spare frame is used. These tests can be run periodically in order to detect stuck-at...
faults. In addition to the ILT method, an improved syndrome storing-based detection (SSD) method is presented to store the results. The system reroutes data of an erroneous frame to a set of spare frames without interrupting the data flow.

This paper is organized as follows. Section II provides the overview of MBU detection and correction. Section III describes the permanent error detection. In section IV results and performance analysis are described. Finally, the paper is concluded in Section V.

II. MULTIPLE BIT UPSET DETECTION AND CORRECTION

The idea behind achieving of MBU detection and correction is to calculate parity of a message, which receivers can be used to check the accuracy of the delivered message and to recover the corrupted data.

A. I3d parity technique

A parity bit, which is added to a string, indicates whether the number of 1-bits in the string is odd or even. The parity bit is the simplest form of error detection technique. There exist some MBU patterns, which affect an even number of cells. The parity techniques other than I3D parity are not efficient to detect such MBU patterns [9]. I3D parity has three set of parity bits such as horizontal, vertical and diagonal. In this technique, each vertical (horizontal) parity bit is obtained by XORing multiple columns (rows). An interleaving group is formed by all columns (rows) which are separated by a constant distance v (h). The bits within an interleaving group are covered by only one vertical (horizontal) bit.

![I3D Parity Technique Diagram](image)

In order to distribute d diagonal parity bits uniformly for a configuration frame of size f * g, it is computed by the equation \([i + f, (j - 1)] \mod d\) where, \((i, j)\) is the bit position. I3D parity provides more detection coverage than other parity techniques. Figure 1 shows an example of the I3D parity technique with the vertical, horizontal, and diagonal interleaving distance of 3, 3, and 4, respectively.

B. Erasure code

Erasure code is a forward error correction (FEC) code which encodes k blocks into n blocks such the original message can be reconstructed from the encoded data [10]-[12].
Erasure code error recovery scheme is used in error correction in caches, storage devices etc. The parity-based optimal erasure code with one redundant block can recover from all the cases with one erased block. In order to reduce the time of error recovery, the configuration frames could be divided into several clusters, each with its own redundant block.

In this scheme, the parity of the configuration frames of the respective cluster is stored in the respective redundant blocks as shown in figure 2. In order for the efficient functionality, the error detection and recovery (EDR) unit periodically performs I3D parity to detect erroneous frames. When an erroneous frame is detected, this unit restores the contents of the erroneous frame according to the contents of remaining frames in the same cluster. The affected frame is assumed to be erased and the contents of the erased block could be simply computed by XORing the bits of the redundant block with the bits of other configuration frames.

The transition errors, as well as the permanent errors in the configuration frames, might affect its functionality. Therefore it is essential to use the techniques which could address permanent errors rather than erasure code which could fix only the transition errors.

C. Power gating

Power gating is a technology that uses a power gate to control the supply to the blocks [13]. Coarse-grained power gating uses an individual power gate (figure 3) for a group of frames.

A power gate includes AND gate and 2:1 multiplexer. The conduction from the AND gate is based on the selection line given. Here, each cluster is provided with a single power gate. During run time if a cluster is not necessary, no supply is given to that particular cluster by giving ‘0’ to the selection line (s). If the selection line is given ‘1’, the output of the multiplexer is ‘1’ and hence the AND gate conducts.

Figure 2. Cluster wise error recovery using erasure code.

Figure 3. Power gate.
III. ADDRESSING OF PERMANENT ERRORS IN CONFIGURATION FRAME

Addressing of permanent errors in configuration frame using spare frames is a two-step process as shown in the flow diagram (figure 4). First, the test vectors are checked against the erroneous configuration frames and the results are stored in a register based block. Second, the results and the input test vectors are compared. If the resultant error is permanent, the data is rerouted to the spare frame.

![Flow diagram](image)

**Figure 4. Flow diagram.**

A. **ILT Method**

The permanent errors that affect the functionality of the mapped design are to detected and corrected during run time. Once an erroneous frame is detected in a cluster using I3D parity technique, the next step is to apply a novel in-line test (ILT) method and a syndrome storing-based detection (SSD) method to determine the type of error. An ILT method is a procedure to test possible patterns of binary bits in order to detect multiple bit upsets that cause the permanent fault. This method mainly checks for the stuck-at-0 and stuck-at-1 faults and can be achieved during normal operation, without interrupting the data.
The test patterns are continuously passed one by one to the erroneous configuration frame to determine the type of error. The main test patterns used are ‘1111111111111111’, ‘0000000000000000’, ‘1010101010101010’, and ‘0101010101010101’.

The results that obtain are stored in SSD. From the results obtained, the type of error can be identified by comparing the results. If the error is a transient error, then the original message can be reconstructed using erasure code. If the error is permanent, then the data is rerouted the spare frame without interrupting the data flow as shown in figure 5. Figure 6 shows a power gate connected to the cluster in order to control the power supply during runtime.
B. SSD method

The basic idea behind SSD is that the information about the errors of erroneous configuration frame is stored in an error syndrome of an error control code. After applying the procedure of ILT, the results of these test patterns are stored in the syndrome. These results are compared with the test patterns. If there exists stuck at faults in the configuration frames, then it can be concluded that there is a permanent error in the cluster.

By using the normal decoding procedure the error location can be extracted from the syndrome. The effectiveness increases from the fact that it takes advantage of the decoder that is already present at the system. To determine how many syndromes to be considered before deciding that an error is permanent is an important design decision for the SSD method. ILT and SSD together perform the addressing of permanent errors by passing the test vectors and by comparing the results.

IV. RESULTS

In this section, the detection and correction of transient, as well as permanent errors, are shown. The entities such as power, area, and delay are also measured.

A. SIMULATION RESULTS

The original data stored is “1111001011110010” and if a fault is detected using I3D parity as shown in figure 7, the test vectors given using ILT method are “1111111111111111”, “0000000000000000”, “1010101010101010” and “0101010101010101”.

![Figure 7. Fault detection.]

If the result of all test vectors given to the erroneous configuration frame is not same then it is a transition error “1111001011110001” and can be corrected using the erasure code as shown in figure 8.

![Figure 8. Reconstruction of transient error.]

If the result of all test vectors given to the erroneous configuration frame is same then it is a permanent error “1111000011110000” and can be corrected by rerouting the bits to a spare frame as shown in figure 9.

![Figure 9. Reconstruction of permanent error.](image)

**B. SYNTHESIS RESULTS**

Power, delay, area, design time and testability are the important parameters to be considered in FPGA design. Among these entities, power and delay values are mainly considered for the proposed design. The power values of the proposed design without and with the use of power gate are shown in figure 10 and figure 11.

![Figure 10. Power without power gate.](image)

![Figure 11. Power with power gate.](image)

The delay values of the proposed design without and with the use of power gate are shown in
figure 12 and figure 13.

### Timing Summary:

**Speed Grade:** -12

- Minimum period: 4.389ns (Maximum Frequency: 227.850MHz)
- Minimum input arrival time before clock: 4.613ns
- Maximum output required time after clock: 4.338ns
- Maximum combinational path delay: 6.804ns

### Timing Detail:

All values displayed in nanoseconds (ns)

*Figure 12. Delay without power gate.*

### Timing Summary:

**Speed Grade:** -12

- Minimum period: 4.389ns (Maximum Frequency: 227.850MHz)
- Minimum input arrival time before clock: 4.613ns
- Maximum output required time after clock: 4.328ns
- Maximum combinational path delay: 6.794ns

### Timing Detail:

All values displayed in nanoseconds (ns)

*Figure 13. Delay with power gate.*

### C. PERFORMANCE ANALYSIS

The total power consumed by the proposed design is less when compared as shown in Table 1. Power and delay values of the proposed design got reduced from the normal value with the use of power gate by shunting the current to the unused blocks during runtime.
Table 1. Comparison of MBU detection and correction schemes

<table>
<thead>
<tr>
<th>Parameters</th>
<th>13d + Erasure code (4 clusters)</th>
<th>13d + (ILT + SSD) Erasure code (4 clusters)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without power gate</td>
<td>With power gate</td>
</tr>
<tr>
<td>Quiescent Power (W)</td>
<td>0.235</td>
<td>0.234</td>
</tr>
<tr>
<td>Dynamic Power (W)</td>
<td>0.098</td>
<td>0.074</td>
</tr>
<tr>
<td>Total Power (W)</td>
<td>0.332</td>
<td>0.308</td>
</tr>
<tr>
<td>Delay (ns)</td>
<td>6.804</td>
<td>6.804</td>
</tr>
<tr>
<td>Frequency (MHz)</td>
<td>327.161</td>
<td>433.614</td>
</tr>
<tr>
<td>Function</td>
<td>Recovery of transient error alone</td>
<td>Recovery of transient as well as permanent error</td>
</tr>
</tbody>
</table>

V. CONCLUSION

Multiple bit upsets which cause temporary and permanent effects in the configuration frames are to be detected and corrected for the efficient functionality of a mapped design. After the detection of error using a low-cost error detection technique, a novel in-line test (ILT) method is used to send the test vectors to the frame for distinguishing between temporary and permanent faults. The results from the frames are stored in the SSD syndrome and compared with the inputs. If it is a temporary fault, the original bits are reconstructed using the erasure code. If it is a permanent fault, the data is rerouted to a spare frame.

The total power consumption of the proposed method is less when compared. The power value again reduced from the normal value when a power gate is connected. The proposed design recovers transient as well as permanent errors.

REFERENCES